Amendment to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listings of Claims

Claims 1-18 (canceled)

Claim 19 (new): A semiconductor intermediate product, comprising:

a semiconductor wafer having a plurality of device surface areas which are separated from one another by scribe lines, wherein each of the device surface areas includes a substrate mounting region and a plurality of surface electrodes adjacent the substrate mounting region;

a plurality of wiring substrates fixed to the substrate mounting region of the plurality of device surface areas, respectively, wherein a peripheral surface region of each of the wiring substrates includes a plurality of electrode pads;

a plurality of wiring bondings which connect the plurality of electrode pads to the plurality of surface electrodes within each of the plurality of device surface areas; and

a resin contained between adjacent wiring substrates so as to cover the scribe lines, the electrode pads, the wiring bonding, and the surface electrodes between the adjacent wiring substrates within the resin.

Claim 20 (new): The semiconductor intermediate product of claim 19, further comprising an insulating adhesive which fixes wherein the plurality of wiring substrates to the substrate mounting region of the respective plurality of device surface areas.

Claim 21 (new): The semiconductor intermediate product of claim 19, wherein the peripheral surface region of each of the wiring substrates is stepped down from a central surface region of each of the wiring substrates, and wherein the resin covers the peripheral surface region of each of the wiring substrates and does not cover the central surface region of each of the wiring substrates.

Claim 22 (new): The semiconductor intermediate product of claim 20, wherein the peripheral surface region of each of the wiring substrates is stepped down from a central surface region of each of the wiring substrates, and wherein the resin covers the peripheral surface region of each of the wiring substrates and does not cover the central surface region of each of the wiring substrates.